RAPIDRFSLUG

RapidRF Smart LDMOS Front-End Designs

A3M36SL039, A3M39SL039

Rev. 1 — January 2023 User Guide

1 Introduction

NXP's RapidRF front-end designs are complete RF front-end solutions for 5G TDD radio systems. They are ideal for transmitters requiring 5 to 10 watts (37–40 dBm) average power with approximately 8.5 dB PAR LTE/NR signals. The designs feature high efficiency Doherty power amplifier multi-chip modules (PAMs) and can be linearized up to 400 MHz instantaneous bandwidth while meeting regulatory emissions requirements when used in conjunction with digital pre-distortion.

The series uses a common PCB layout, simplifying both design and manufacturing.

2 System description

On the Tx path, the RapidRF designs integrate a pre-driver multi-chip module driving a Doherty RF power amplifier module connected through a circulator to the antenna port. The Tx path sufficiently amplifies low-level signals (≤ 10 dBm) from the RF modulator output up to full antenna output power. Tx output coupling is provided for wideband RF feedback required for digital pre-distortion (DPD). On the Rx path, the same antenna port and circulator feed into the Rx front-end dual channel module. Receive front-end module includes a high-speed, high power switch ahead of a low noise, high intercept point amplifier.

TDD operation is controlled by simple logic levels on 2 pins, one to enable the power amplifier and the other to enable the receive sub-system and control the integrated switch. Bias settings are factory preprogrammed and do not need to be adjusted.

Contents

2.1 Key specifications

Table 1. Tx path (uncorrected configuration)

Frequency (MHz)	Average Power (dBm)	Gain (dB)	Efficiency (%)	PAR (dB)	V_{DD} (V)	RapidRF Front-End Design Board Part Number
3400–3800	39	54	33	7.5	29	RAPIDRF-36SL039
3700–4000	39	53	30	7.5	30	RAPIDRF-39SL039

Table 2. Rx path

Frequency (MHz)	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	OIP3 (dBm)	RapidRF Front-End Design Board Part Number
3400–3800	30[1], 36[2]	1.6[2], 1.9[1]	–8[1], –13[2]	23	RAPIDRF-36SL039
3700–4000	30[1], 36[2]	1.5[2], 1.8[1]	–8[1], –13[2]	23	RAPIDRF-39SL039

1. Low gain mode
2. High gain mode

Table 3. Power supply requirements

Current Consumption (mA)			V_{DD} Output Stage Voltage	RapidRF Front-End Design Board Part Number
5 V Rx	5 V Tx	Tx Output		
65	115	800	29	RAPIDRF-36SL039
65	115	880	30	RAPIDRF-39SL039

2.2 Block diagram

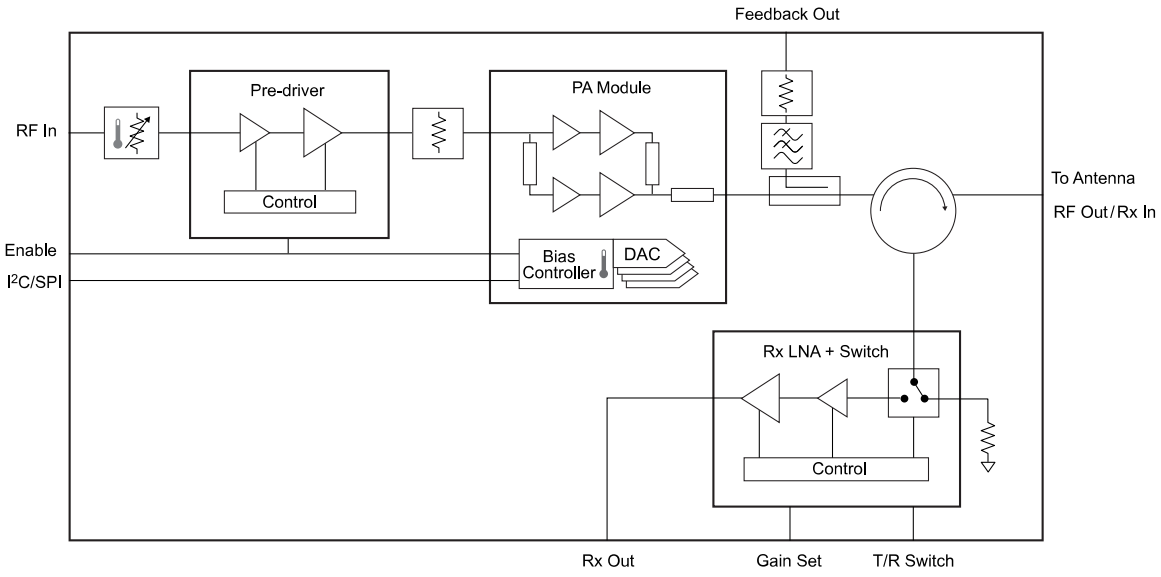


Figure 1. RapidRF smart LDMOS front-end design block diagram

3 System design theory

3.1 Tx pre-driver multi-chip module

The pre-driver integrated circuit is designed for an input signal level of approximately –20 dBm and an output power of approximately 13 dBm. These are average powers with expected PAR (peak-to-average ratio) of approximately 10 dB. The pre-driver is operated in class A or AB linear to simplify error correction. The input to the pre-driver is passed through a temperature sensitive attenuator to stabilize gain over temperature. The output is routed through a 2 dB attenuator that provides improved isolation and match to the integrated PAM.

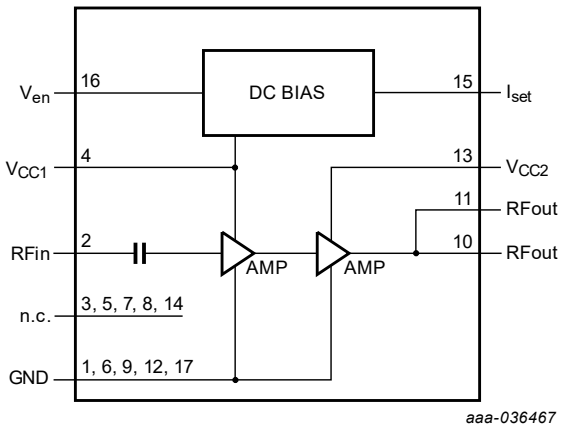


Figure 2. Functional block diagram — BTS6201U

3.2 Power amplifier multi-chip module

The PAM is a two-stage Doherty amplifier. Both the input and output are matched to 50 ohms, simplifying layout and design complexity. Bias for the devices in the PAM are individually programmed for precise control of the quiescent currents. The bias is temperature compensated. The preprogrammed bias settings can be overridden through the I^2C control port. The amplifier output is sampled by a 38 dB coupler ahead of the circulator to provide a wideband DPD feedback signal. The through path from the coupler is connected to the antenna port through a circulator.

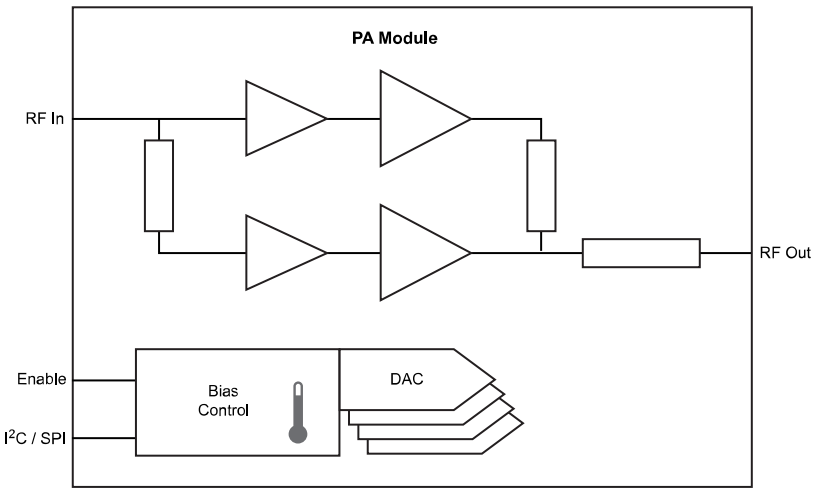


Figure 3. Functional block diagram — A3M36SL039/A3M39SL039

3.3 Receive switch/LNA module

The receive pre-amplifier is connected to the antenna port through the circulator and switch. The switch protects the pre-amplifier from over load when transmitting. The pre-amplifier has a low noise figure, a high intercept point and wide bandwidth.

For situations where higher power handling is needed, gain can be reduced by 6 dB with minimal impact to noise figure.

The BTS7203U is a dual channel device, but in this application only one channel is used.

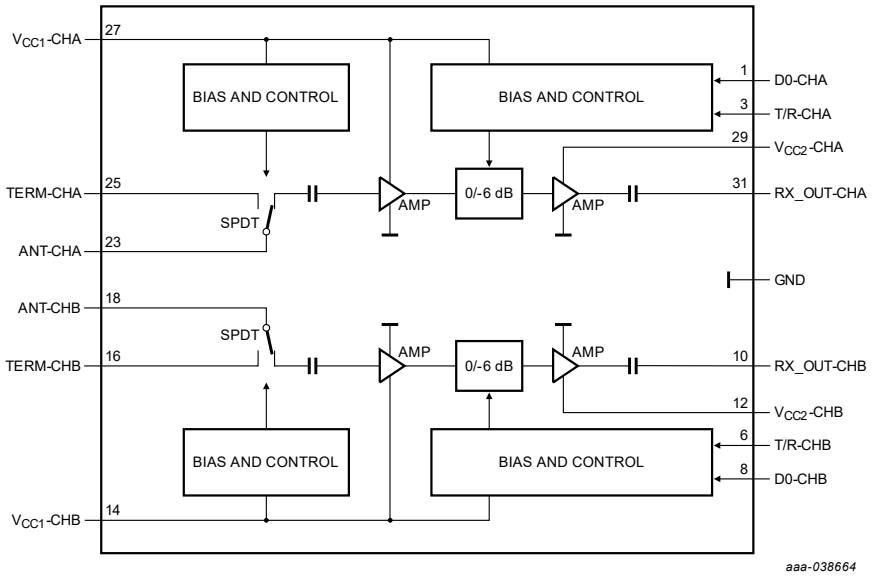


Figure 4. Functional block diagram — BTS7203U

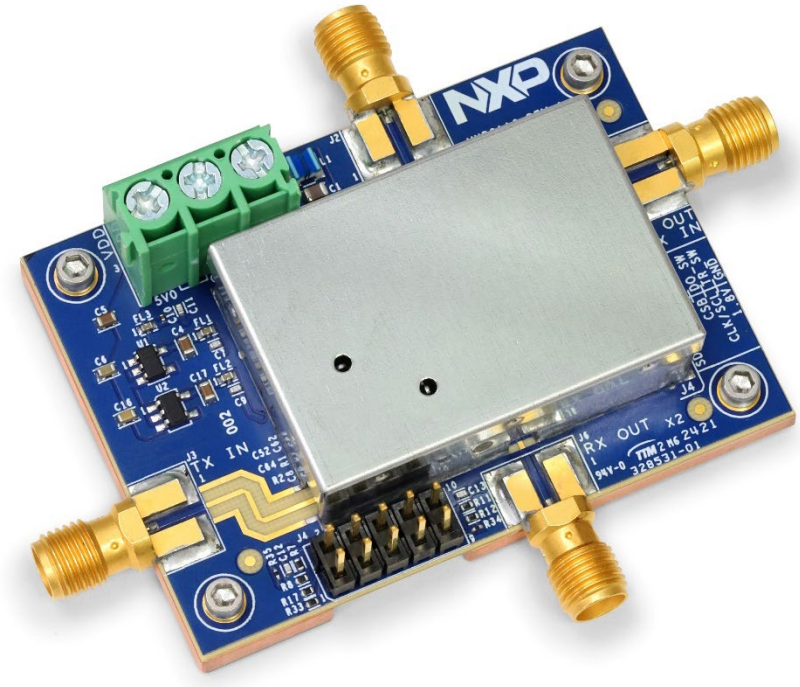


Figure 5. RapidRF smart LDMOS front-end design — A3M36SL039/A3M39SL039

3.4 Circulator

The circulator provides both a stable impedance for the transmitter and low loss path to the receiver, minimizing noise. In transmit mode the circulator isolation port is connected through the switch to a termination. In receive mode the isolation port is connected through the switch to the low noise amplifier (LNA).

4 Hardware testing and setup

4.1 Required hardware and software

4.1.1 Power supplies

4.1.1.1 24–32 V, 1 A regulated power supply

The PSU should be either high speed or well decoupled at the device as there are significant current spikes in normal operation. A 1000 µF aluminum electrolytic capacitor is recommended.

4.1.1.2 5 V, 250 mA regulated power supply

This power supply is for the bias controller and the linear regulators that supply pre-driver and receiver functions.

4.1.2 Heatsink

The RapidRF board will dissipate up to 15 W in normal operation. The heat spreader included is not adequate to dissipate such power. A suitable heatsink must be attached to the heat spreader with a thermal interface material like silicone thermal compound.

A recommended heatsink is a 78 mm^2 × 36 mm high heatsink from Mersen. Many other configurations are possible.

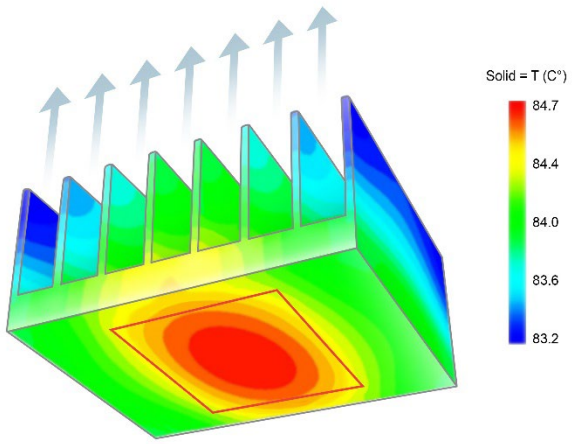


Figure 6. Thermal example (40°C ambient convection only)

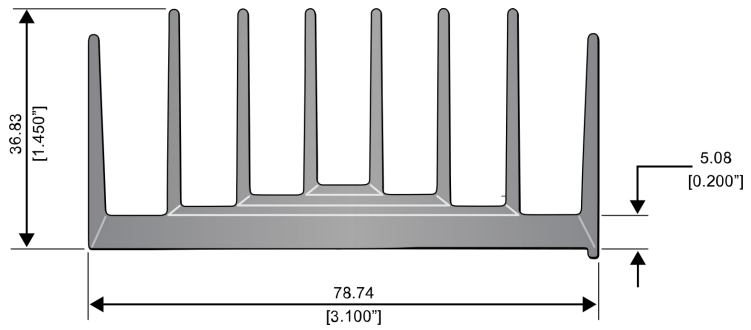


Figure 7. Example heatsink

4.1.3 Transmit receive and PA enable control

For static testing jumpers may be used between control pins and the 1.8 V pin on the control connector.

Logic levels for external controls must not exceed 2 V and cannot be clamped to the 1.8 V pins.

NOTE

Care must be taken to ensure that transmit power is not applied when the Transmit/Receive switch is in Receive mode (logic low on control pin). Failure to do so may cause destruction of the pre-amplifier module.

4.2 Pinout function

Table 4. J4 control connector

Pin	Name	Function	Limits
1	SDA/SDIO	SPI or I^2C data for bias controller programming [1]	1.8 V logic 2.0 V max, pulled high
2	PA Enable	0 = PA Standby, 1 = PA Enable	1.8 V logic 2.0 V max, pulled low
3	N.C.	—	—
4	1.8 V internal	—	1 mA sink or source max
5	CS_B	SPI chip select, active low [1]	1.8 V logic 2.0 V max, pulled high
6	D0_SW	Rx gain select 0 = high gain 1 = low gain	1.8 V logic 2.0 V max, pulled low
7	SCL/CLK	SPI or I^2C clock for bias controller programming [1]	1.8 V logic 2.0 V max, pulled high
8	Transmit/Receive switch	0 = Receive mode 1 = Transmit mode	1.8 V logic 2.0 V max, pulled high
9	1.8 V internal	—	1 mA sink or source max
10	Ground	Ground	—

1. Default mode is I^2C with a 7-bit address of 1000 011. See Section 4.6 for alternate I^2C addressing.

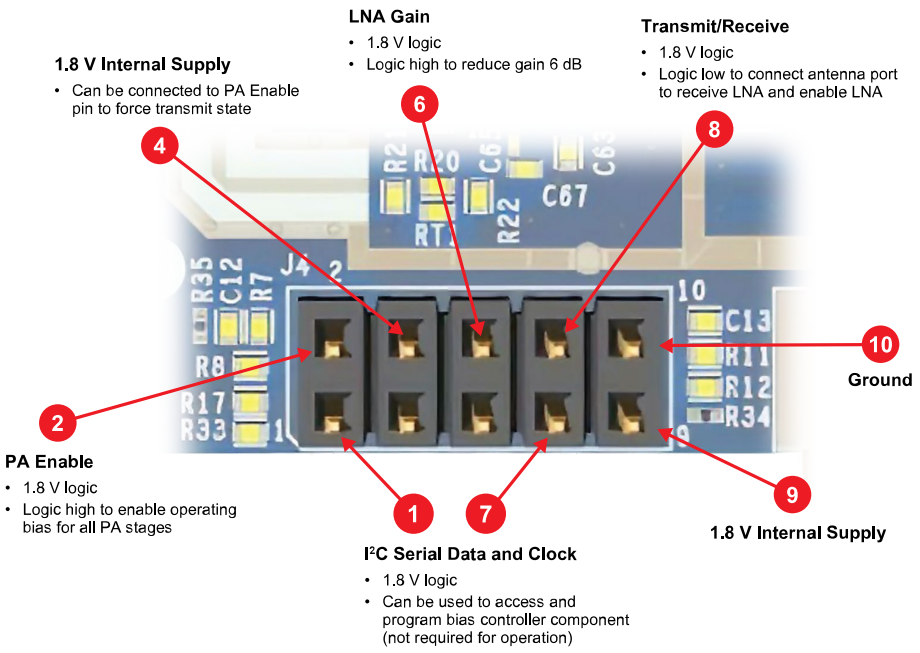


Figure 8. J4 control connector

Table 5. J1 power connector

Pin	Name	Function	Limits
1	V_{DD}	Output stage power supply	32 V max, 1000 mA max
2	Ground	Ground	—
3	5 V	Power supply for logic, receive and pre-driver	5.25 V max, 250 mA max

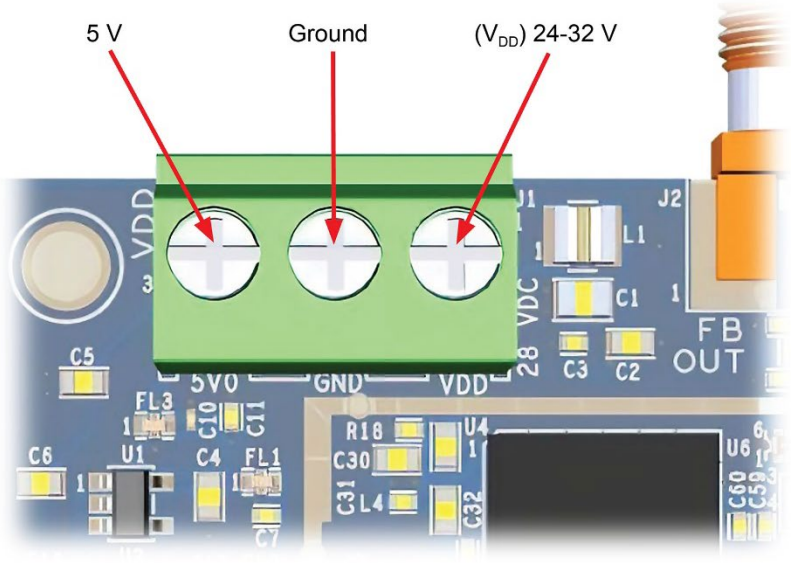


Figure 9. J1 power connector

Table 6. RF connections

RF Jack	Name	Function	Limits
J2	FB out	Feedback for DPD, from PA, before circulator or filter	~38 dB below RF output level
J3	Tx in	Transmit signal in	Max 0 dBm peak, –10 dBm Avg.
J5	Tx out	Transmit/Receive antenna port	–15 dBm max Receive, +39 dBm Transmit
J6	Rx out	Receive signal out	—

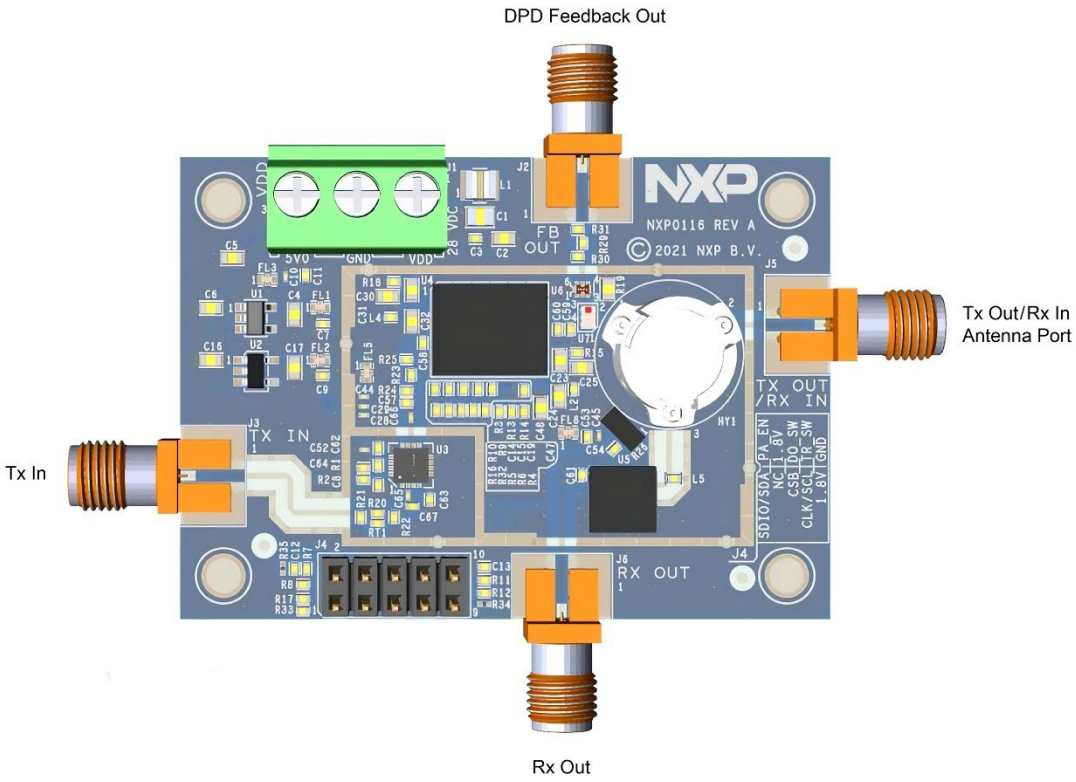


Figure 10. RF connections

4.3 Testing setups

4.3.1 Power sequencing

Be sure to put the RapidRF board in Standby mode, with both Transmit and Receive modes disabled before applying power.

For Transmit power down, remove the RF signal and put it in Receive mode prior to removing either power supply.

The power supply sequence in Receive mode is not critical.

4.3.2 Setting bias

Bias controller is preprogrammed; therefore, setting of idle current is not necessary.

NOTE

Consult NXP applications for information on bypassing preprogrammed bias settings.

4.3.3 Receive test setup

1. Mount RapidRF board on heatsink.
2. Float or connect the PA Enable terminal to ground.
3. Connect the TR switch terminal to 0 V (via a jumper or external supply).
4. Set the signal generator to -100 dBm and then disable RF.
5. Connect Tx Out/Rx In antenna port through coupler to attenuator.
6. Connect the signal generator to the coupler forward power port (see Setup figure).
7. Connect the analyzer to the Rx output port (see Setup figure).
8. Connect the 5 V power supply.
9. Turn on the 5 V power supply and note the current. It should be ~100 mA. If not, check the TR switch pin status.
10. Turn on the signal generator and slowly raise the power until the desired output is reached, taking care not to exceed -15 dBm.

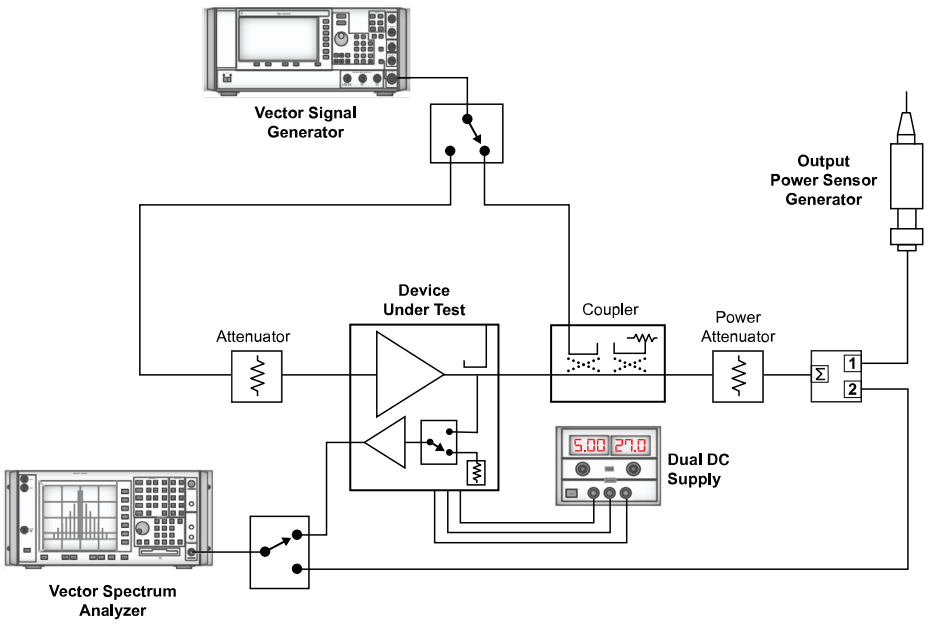


Figure 11. Receive test setup

4.3.4 Transmit test setup

1. Mount RapidRF board on a heatsink capable of dissipating up to 15 W.
2. Set the signal generator to –50 dBm, or less, and then disable RF.
3. Connect the signal generator to Tx In of the RapidRF board (see Setup figure).
4. Connect Tx/Rx In port to through coupler to 10 W attenuator (see Setup figure).
5. Terminate the Rx Output port and Feedback Out port.
6. Connect the 5 V power supply.
7. Float or connect the TR switch terminal to 1.8 V.
8. Connect the V_{DD} (24–32 V) power supply.
9. Turn on the 5 V power supply and note current. It should be less than 70 mA. If ~100 mA check TR switch status. Pin voltage should be less than 0.1 V.
10. Turn on the V_{DD} power supply. The initial current should be close to 0 mA.
11. Connect the PA Enable terminal to 1.8 V (via a jumper or external supply).
12. Check the V_{DD} power supply current. It should be less than 100 mA.
13. Turn on the signal generator and slowly raise power taking care never to exceed –15 dBm average power after input attenuator until the desired output is reached.

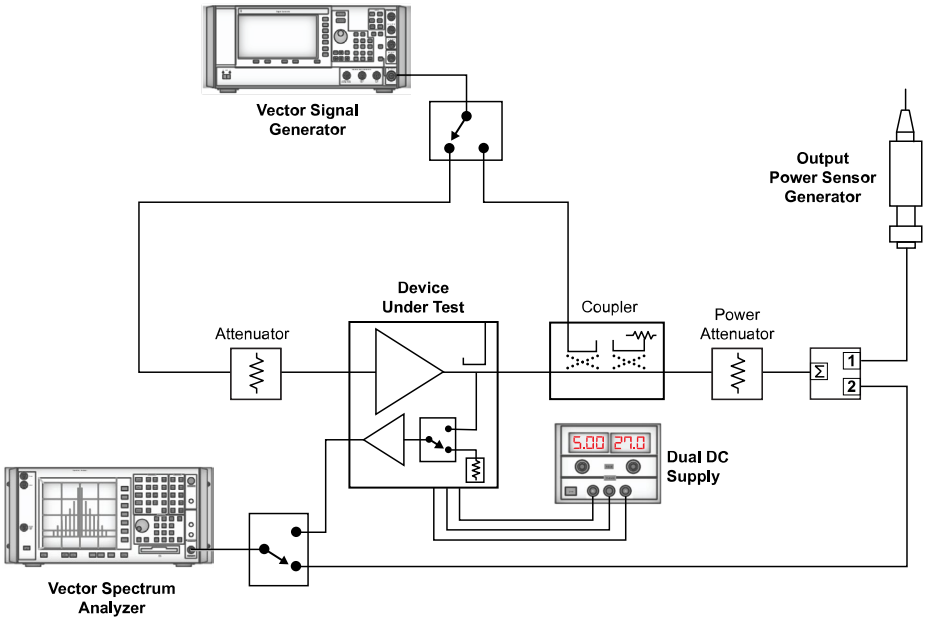


Figure 12. Transmitter test setup

4.3.5 Feedback test setup

1. Mount RapidRF board on a heatsink capable of dissipating up to 15 W.
2. Set the network analyzer output to –50 dBm, or less, after input attenuator.
3. Connect the signal generator to Tx In of the RapidRF board (see Setup figure).
4. Connect Tx/Rx In port to through coupler to 10 W attenuator (see Setup figure).
5. Terminate Rx Output port and Feedback Out port.
6. Connect the 5 V power supply.
7. Float or connect TR switch terminal to 1.8 V.
8. Connect the V_{DD} (24–32 V) power supply (depending on model of RapidRF).
9. Turn on the 5 V power supply and note current. It should be less than 70 mA. If ~100 mA check the TR switch status. Pin voltage should be less than 0.1 V.
10. Turn on the V_{DD} power supply. The initial current should be close to 0 mA.
11. Connect the PA Enable terminal to 1.8 V (via a jumper or external supply).
12. Check the V_{DD} power supply current. It should be less than 100 mA.
13. Turn on the signal generator and slowly raise the power until the desired output is reached taking care to never exceed –15 dBm average power.

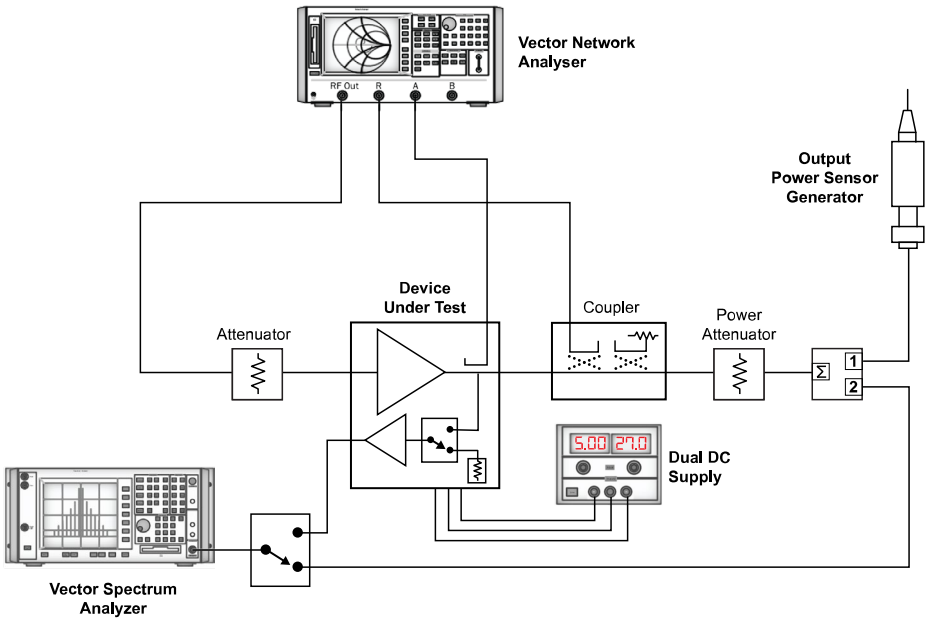


Figure 13. Predistortion feedback test setup

4.4 Software setup

Only the PAM bias controller is accessed through the I²C data interface port. It is not necessary to use the I²C interface for normal operation as the PAM is preprogrammed at the factory for optimal bias settings under standard conditions. Temperature information can be read from port and preprogrammed bias settings can be overridden in Engineering mode. Programming and register details are provided in the corresponding PAM data sheet.

4.5 Physical layer

I²C with 1.8 V logic levels is the default interface. There are internal 4.7k pull up resistors on the port pins. Maximum speed on the interface is 400 kHz. The SPI interface is disabled on the RapidRF board.

4.6 I²C addressing

The I²C address can be changed by populating resistors as shown in Table 7.

Table 7. I²C address assignment

Address	R9	R10	R16	R32
1000 000	x	1k	x	x
1000 001	x	1k	x	1k
1000 010	1k	x	x	x
1000 011 (default)	x	x	x	x
1000 100	x	x	x	1k
1000 101	1k	x	1k	x
1000 110	x	x	1k	x
1000 111	x	x	1k	1k

Note: x = do not populate.

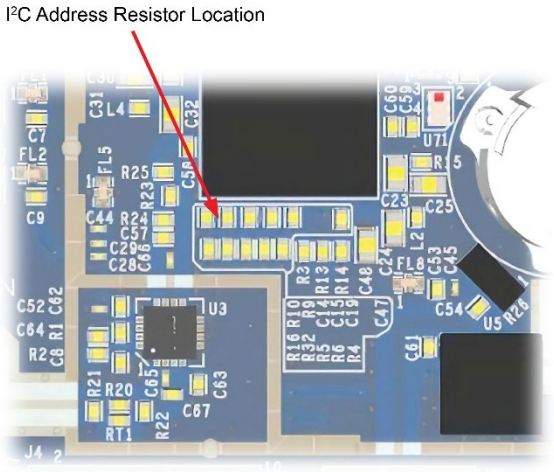


Figure 14. I²C address resistor location

5 Products, design files and software

Table 8. Related products

Product	Description	Link/how to access
A3M36SL039	Module: small footprint 2-stage LDMOS Doherty amplifier with integrated matching	nxp.com/A3M36SL039
A3M39SL039	Module: small footprint 2-stage LDMOS Doherty amplifier with integrated matching	nxp.com/A3M39SL039
BTS6201U	Pre-driver: wideband, high linearity, pre-driver amplifier	nxp.com/BTS6201U
BTS7203U	Rx/switch: dual channel receiver analog front-end module integrating switch and LNA	nxp.com/BTS7203U

Table 9. Design files

Files	Link/how to access
Board layout	nxp.com/RapidRFSL > Design Resources > Design Tools & Files
Schematic	
Board parts list	
Mechanical drawings	

Table 10. Software

Files	Link/how to access
PC-based GUI and adapter	Consult NXP applications for PC-based GUI and adapter that can operate controls and access bias controller registers.

6 Revision history

The following table summarizes revisions to this document.

Table 11. Revision history

Revision	Date	Description
0	May 2022	• Initial release of user guide
1	Jan. 2023	• Updated to include performance information for RAPIDRF-39SL039 Front-End Design board • Table 1, Tx path (uncorrected configuration) RAPIDRF-36SL039: updated gain, efficiency and PAR to reflect measured data, p. 1 • Table A-1, Transmitter uncorrected: updated table to reflect measured data, p. 14

Appendices

Appendix A — A3M36SL039 RapidRF front-end design performance

Transmitter

Typical performance data for RapidRF A3M36SL039 board:

Table A-1. Transmitter uncorrected

Frequency (MHz)	Input Power (dBm)	Output Power (dBm)	Gain (dB)	Efficiency (%)	PAR (dB)	V_{DD} (V)	I_{DD} (A)	5 V CTRL (mA)
3400	–16.5	39.0	55.4	35.8	8.8	29.0	0.76	86
3500	–15.6	39.0	54.6	36.6	8.3	29.0	0.75	86
3600	–15.0	39.0	54.0	34.5	7.8	29.0	0.92	86
3700	–15.5	39.0	54.5	33.5	7.5	29.0	0.82	86
3800	–15.1	39.0	54.1	33.8	7.7	29.0	0.81	86

Table A-2. Transmitter DPD performance

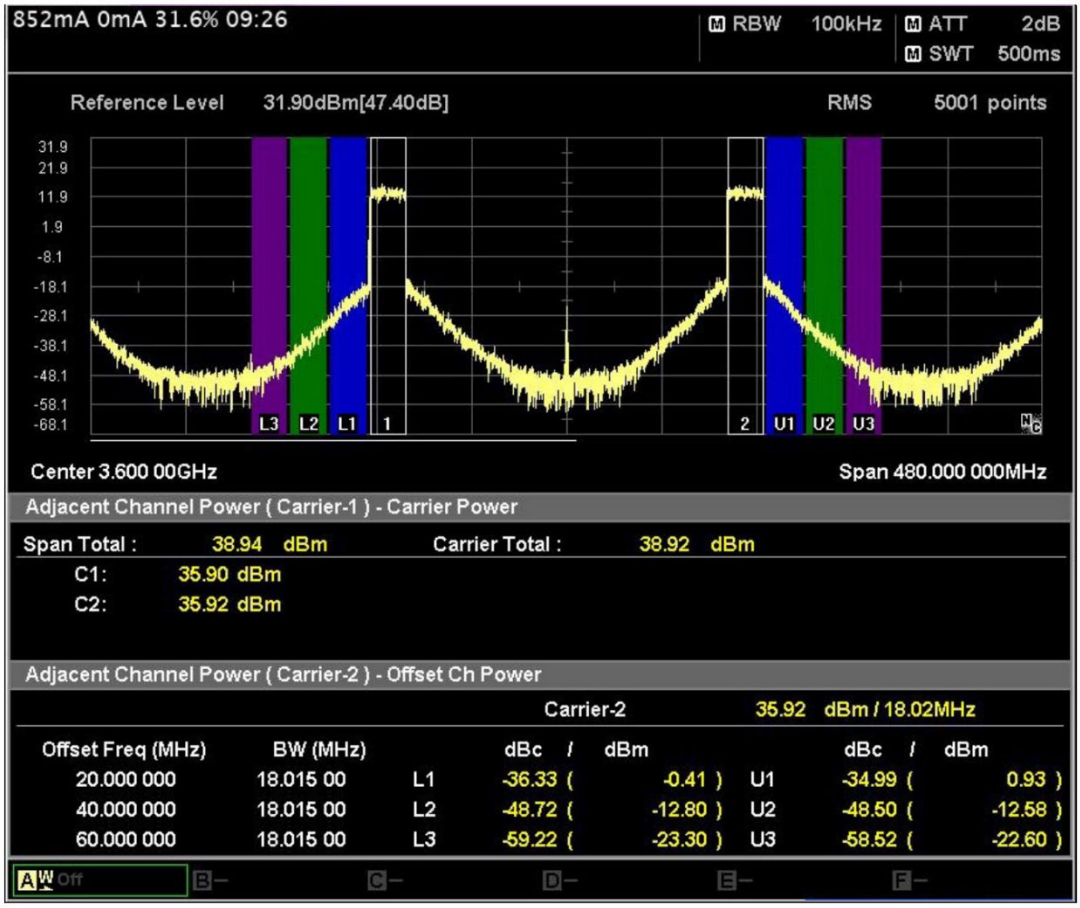
Frequency (MHz)	Signal	PAE (%)	Output Power (dBm)	ACP-L (dBc)	ACP-U (dBc)
3500	1 x 20 LTE @ 7.5 dB PAR	32.4	39.0	–54.9	–55.1
3600	1 x 20 LTE @ 7.5 dB PAR	32.5	39.0	–59.2	–58.9
3700	1 x 20 LTE @ 7.5 dB PAR	31.2	39.0	–49.8	–49.8
3500	2 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	32.0	39.0	–52.7	–52.7
3600	2 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	31.5	39.0	–54.2	–56.4
3700	2 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	30.5	39.0	–51.5	–54.1
3500	10 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	32.0	39.0	–48.1	–48.5
3600	10 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	30.7	39.0	–49.9	–49.2
3700	10 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	29.0	39.0	–49.7	–49.3

39 dBm output power, 32.9% efficiency, 3600 MHz

Figure A-1. Output spectrum, uncorrected (20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)

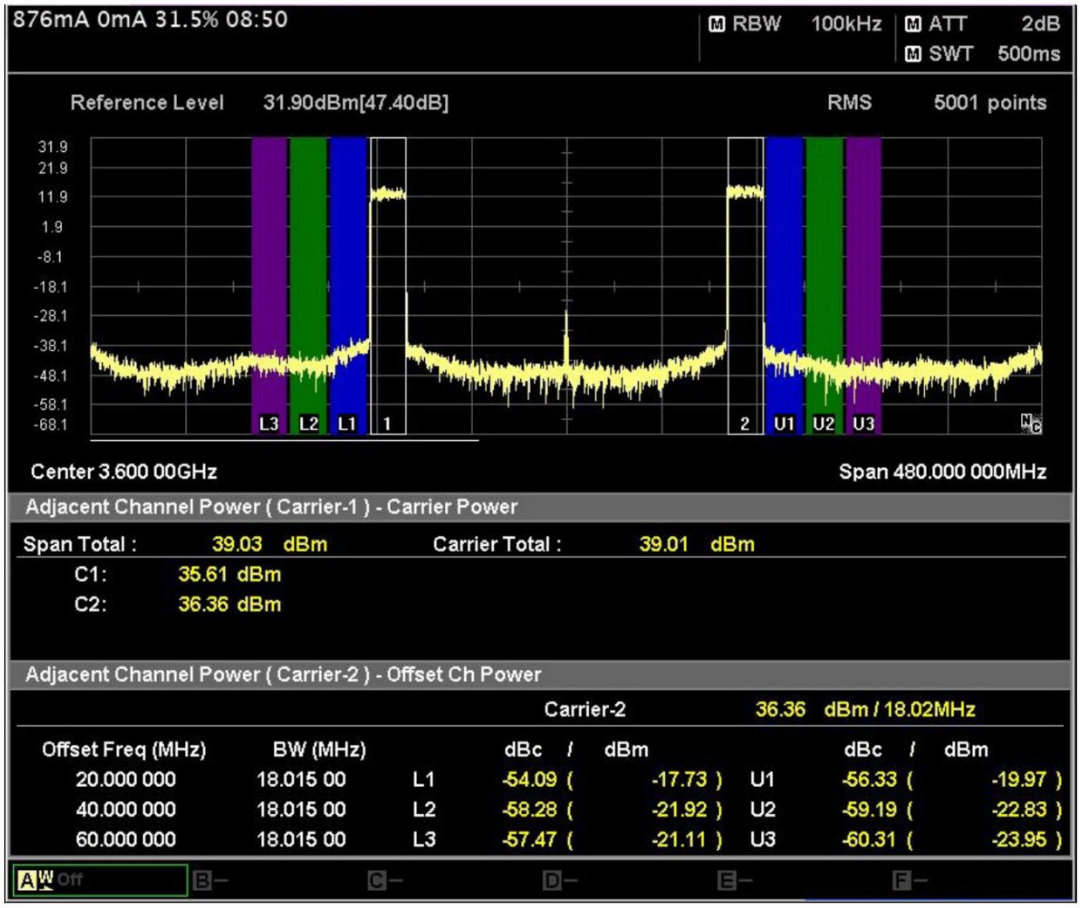
39 dBm output power, 32.5% efficiency, 98 coefficients, 120 Rx filter, 3600 MHz

Figure A-2. Output spectrum, corrected (20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)



39 dBm output power, 31.6% efficiency, 3600 MHz

Figure A-3. Output spectrum, uncorrected (2 × 20 MHz LTE, 7.5 dB PAR, 200 MHz, IBW)

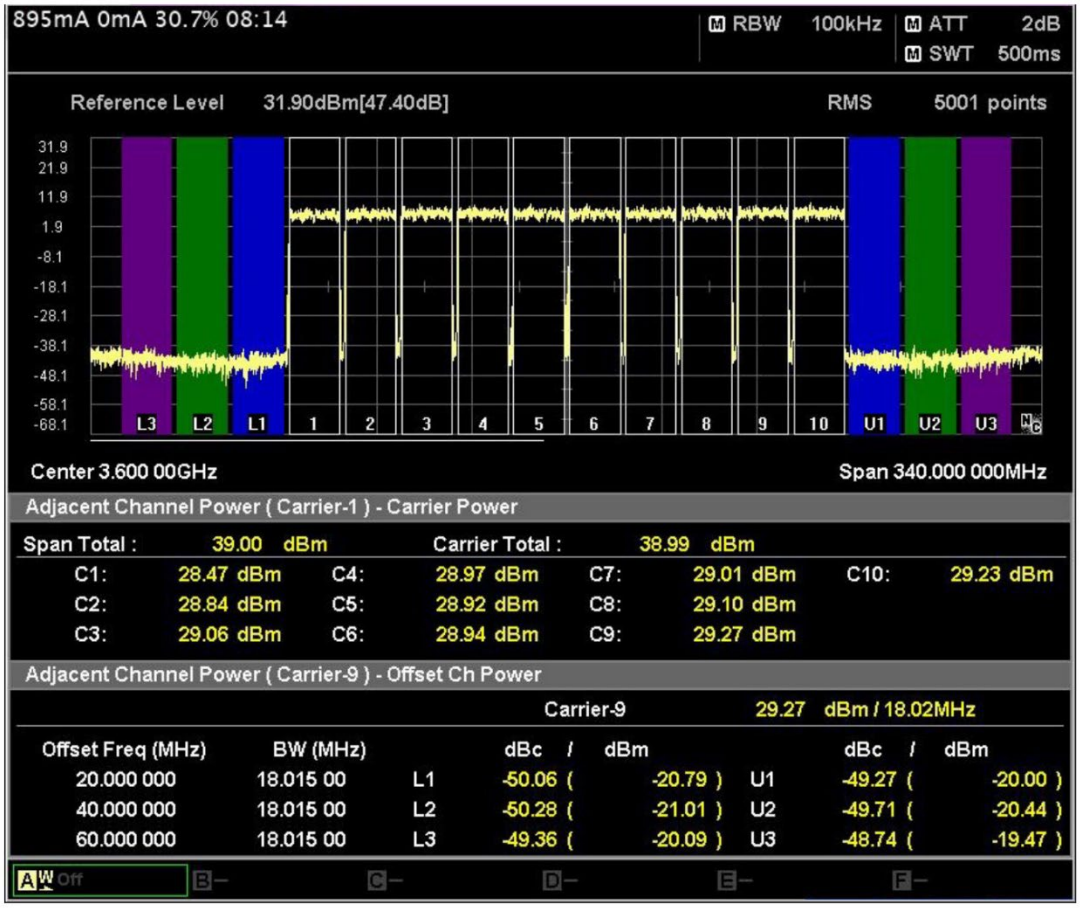


39 dBm output power, 31.5% efficiency, 98 coefficients, 400 Rx filter, 3600 MHz

Figure A-4. Output spectrum, corrected (2 × 20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)

39 dBm output power, 30.8% efficiency, 3600 MHz

Figure A-5. Output spectrum, uncorrected (10 × 20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)



39 dBm output power, 30.7% efficiency, 98 coefficients, 340 Rx filter, 3600 MHz

Figure A-6. Output spectrum, corrected (10 × 20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)

Receiver

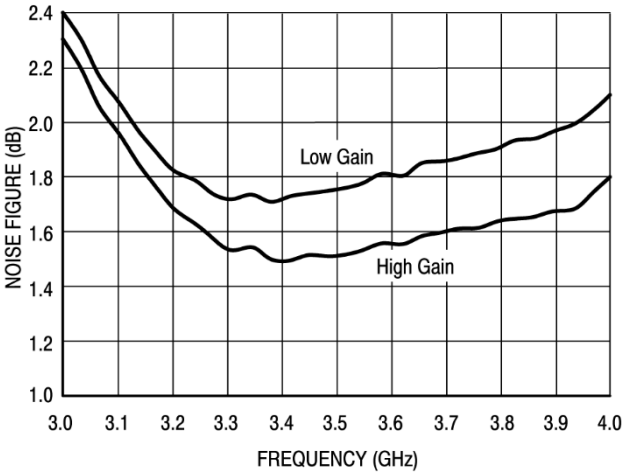


Figure A-7. Noise figure versus frequency

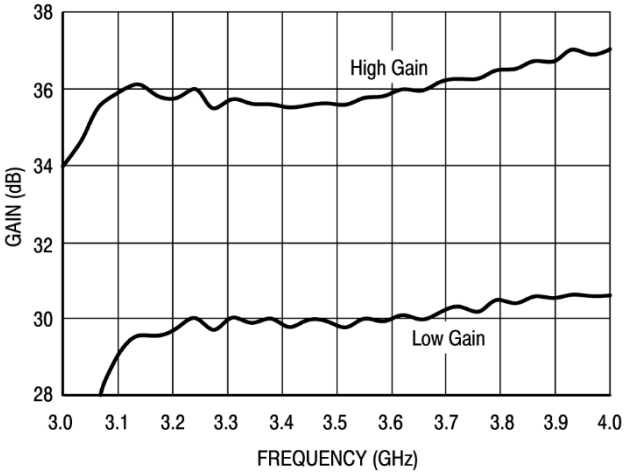


Figure A-8. Gain versus frequency

Appendix B — A3M39SL039 RapidRF front-end design performance

Transmitter

Typical performance data for RapidRF A3M39SL039 board:

Table B-1. Transmitter uncorrected

Frequency (MHz)	Input Power (dBm)	Output Power (dBm)	Gain (dB)	Efficiency (%)	PAR (dB)	V_{DD} (V)	I_{DD} (A)	5 V CTRL (mA)
3710	–15.1	39.0	54.0	31.9	7.8	30.0	0.83	88
3840	–14.4	39.0	53.4	30.7	7.7	30.0	0.86	88
3970	–14.0	39.0	53.0	29.9	7.5	30.0	0.88	88

Table B-2. Transmitter DPD performance

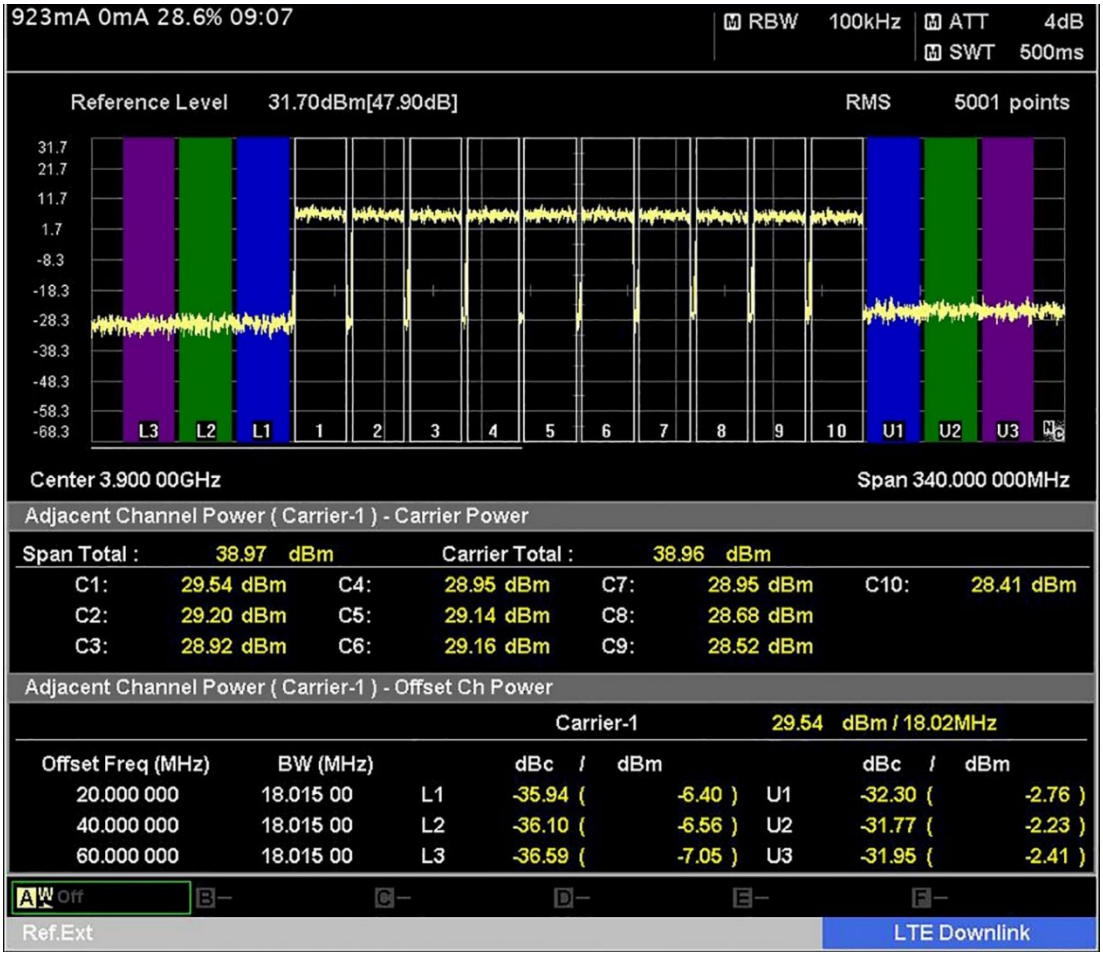
Frequency (MHz)	Signal	PAE (%)	Output Power (dBm)	ACP-L (dBc)	ACP-U (dBc)
3800	1 x 20 LTE @ 7.5 dB PAR	29.8	38.9	–60.5	–60.3
3900	1 x 20 LTE @ 7.5 dB PAR	28.0	38.9	–58.0	–58.7
3800	10 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	29.5	39.0	–52.5	–52.4
3900	10 x 20 LTE @ 7.5 dB PAR, 200 MHz IBW	28.5	38.9	–51.7	–51.3

39 dBm output power, 28.2% efficiency, 3900 MHz

Figure B-1. Output spectrum, uncorrected (20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)

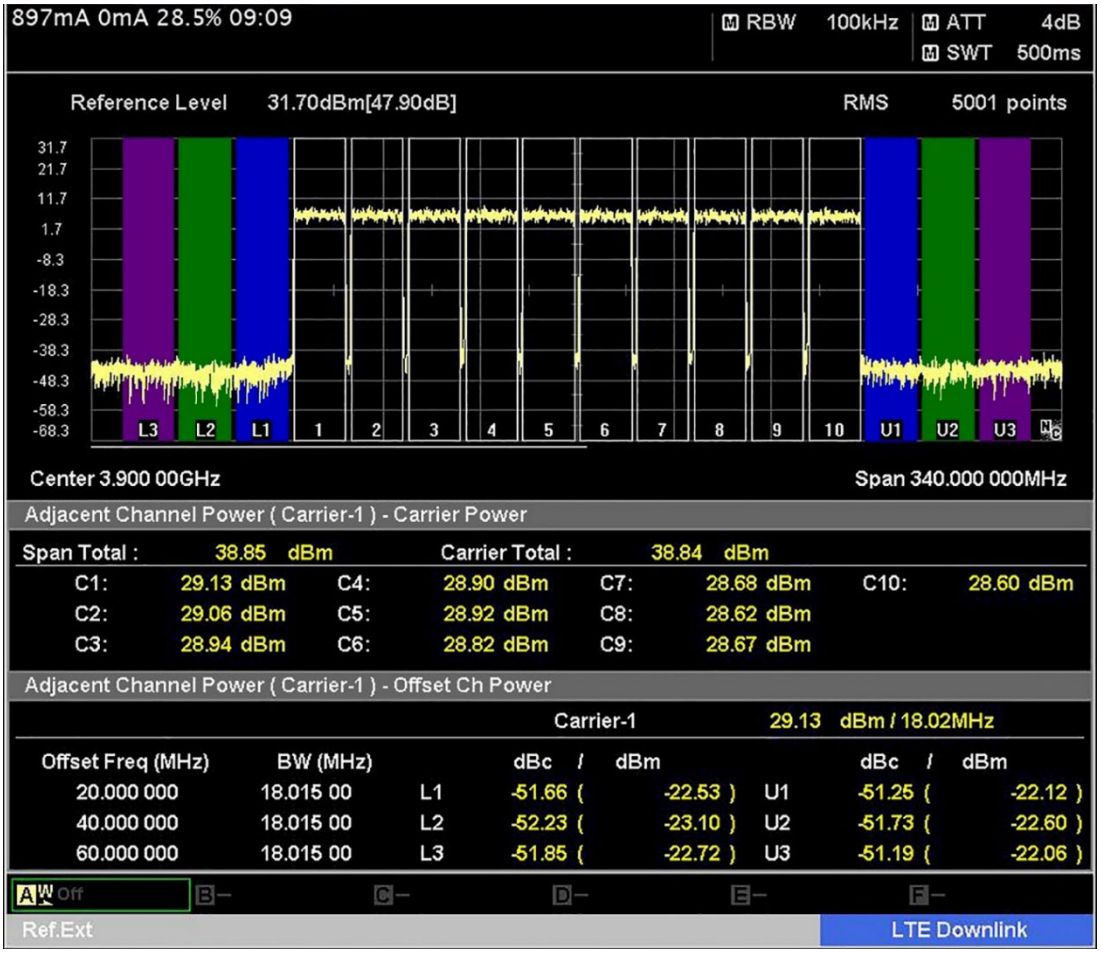
39 dBm output power, 28.0% efficiency, 3900 MHz

Figure B-2. Output spectrum, corrected (20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)



39 dBm output power, 28.6% efficiency, 3900 MHz

Figure B-3. Output spectrum, uncorrected (10 × 20 MHz LTE, 7.5 dB PAR, 200 MHz, IBW)



39 dBm output power, 28.5% efficiency, 98 coefficients, 400 Rx filter, 3900 MHz

Figure B-4. Output spectrum, corrected (10 × 20 MHz LTE, 7.5 dB PAR, 200 MHz IBW)

Receiver

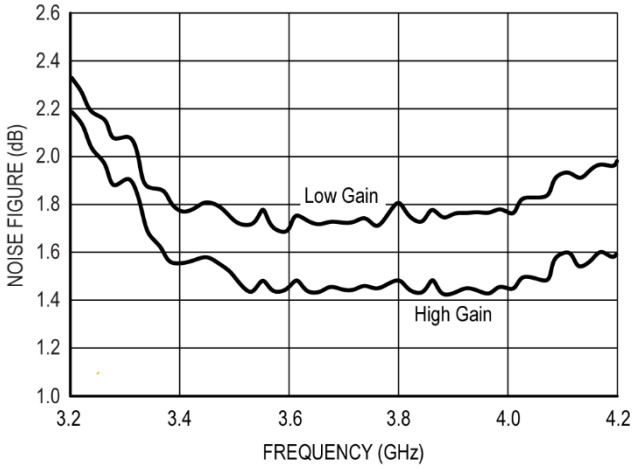


Figure B-5. Noise figure versus frequency

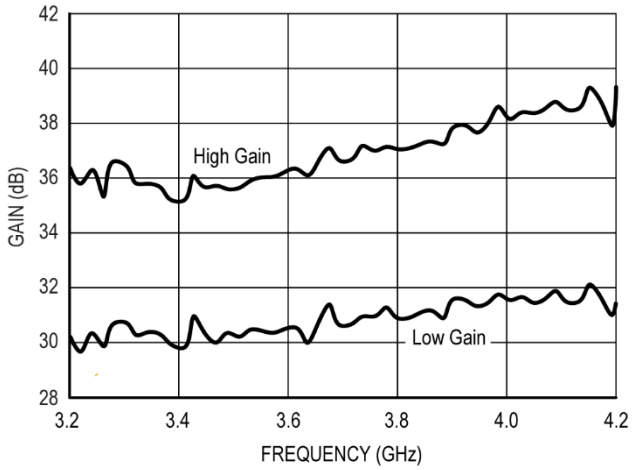


Figure B-6. Gain versus frequency

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