HIGH-VOLTAGE BMS REFERENCE DESIGN

Robust and reliable analog solutions

NXP HVBMS reference design is a scalable ASIL D architecture for high-voltage applications, composed of three modules: Battery Management Unit (BMU), Cell Monitoring Unit (CMU) and Battery Junction Box (BJB).

THE NXP HVBMS REFERENCE DESIGN OFFERS A SOLUTION FOR:

Battery Management Unit (BMU):
The BMU board features the recently launched automotive safety integrity level (ASIL) D S32K3 microcontroller family with at least two cores running in lockstep configuration. The MCU and the rest of components in the BMU board are powered by the FS26 SBC to achieve ASIL D at system level and a robust power management of the board.

For battery-internal communication, the HVBMS reference design offers two possible architectures: isolated electrical transport protocol link (ETPL) or CAN/CAN FD.

Cell Monitoring Unit (CMU):
The CMU board features four of our latest ASIL D compliant battery cell controllers (BCC), together monitoring and balancing up to 56 cells. For a highly optimized bill of material (BOM) the on-board communication is isolated using capacitive coupling. Multiple boards can be daisy-chained to extend the battery cell count to target up to 800 V systems.

Battery Junction Box (BJB):
The BJB board features two of our latest MC33772C ICs redundantly measuring battery pack current and several high voltages. The BJB also performs Coulomb Counting without MCU interaction to enable highly accurate state of charge and state of function calculation.

KEY GENERAL FEATURES

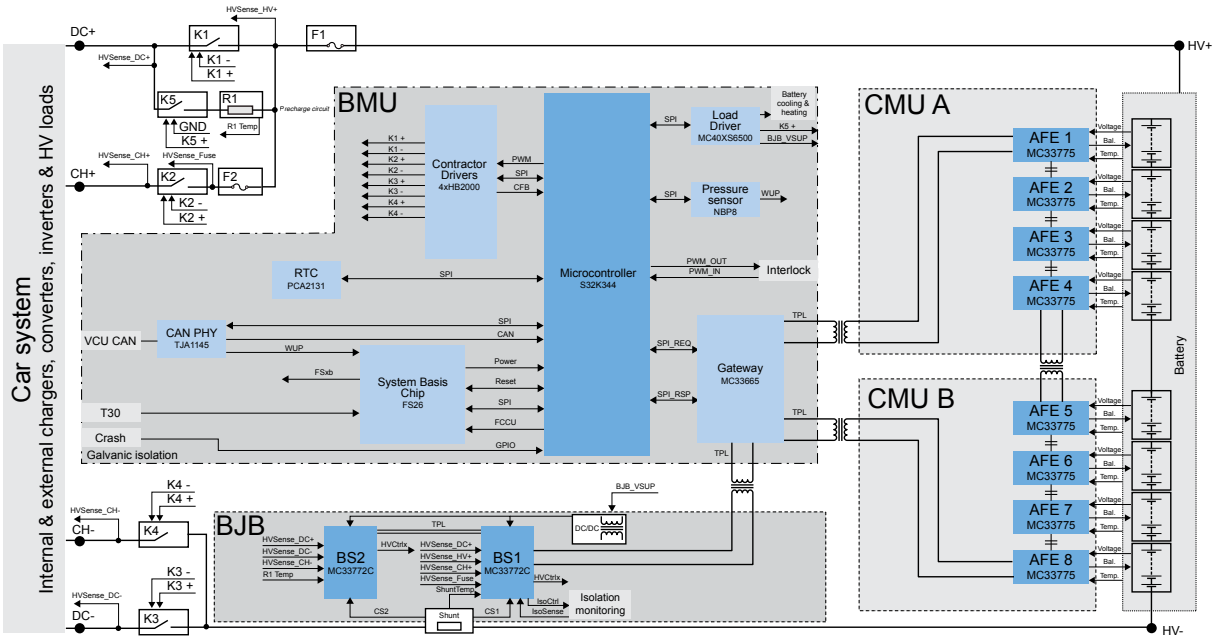
- Scalability: High-voltage BMS chip set solutions for a wide range of applications to reduce development cost and enable faster time to market.
- Safety: High system safety level ensures proper operation of the battery at all times, protecting the passengers.
- Precision: Precise and synchronized measurements enable to leverage the full potential of the battery thus maximizing driving range.

TARGET APPLICATIONS

- Automotive and industrial high-voltage battery management

BMU	**Interfaces**	• 3x CAN FD interfaces, one with partial networking • 4x TPL interfaces • 4x contactor drivers with PWM economization and current monitoring • 2x overcurrent protected outputs for battery cooling/heating valves • 2x overcurrent and reverse polarity protected outputs for junction box and DC-Link bus pre-charge contactor
	Advanced Features	• On board pressure sensor for thermal runaway detection • PWM-based interlock pilot loop • Lower current consumption in sleep mode • Cell voltage and battery current measurement synchronization for state of health calculation
	Wake-Up Sources	• SBC – periodic wake-up • VCU CAN – partial networking • CMU wake-up via CMU CAN/CAN FD or ETPL • Pressure sensor – thermal runaway event detection
CMU	**Voltage Measurement**	• 4 x 14 channel BCCs for up to 56 cells, extendable by adding more CMUs to the daisy chain • Life-time guaranteed high accuracy cell voltage measurement channels, with averaging and advanced filtering
	Temperature Measurement	• 4 x 8 analog inputs (including temperature sensors) or GPIOs with advanced filtering
	Cell Balancing	• Cell balancing with integrated temperature-controller function with up to 300 mA (100 mA using default setup)
	Communication	• Isolated ETPL communication between CMU and BMU
BJB	**High-Voltage Measurement**	• 7 high voltage measurements with high accuracy
	Battery Current Measurement	• Fully redundant current measurement up to +/-1500 A (with populated shunt, adaptable) • 0.5% measurement error (IC level only)
	Temperature Measurement	• Shunt temperature measurement for current measurement compensation • Pre-charge resistor temperature measurement
	Isolation Measurement	• Isolation resistance measurement between high voltage and low voltage domains
	Communication	• Isolated ETPL communication between BJB and BMU

HVBMS 400 V ETPL ARCHITECTURE



ENABLEMENT TOOLS

- Development Hardware:
  - BMU board: NXP.com/RD-K344BMU
  - CMU board: NXP.com/RD33775ACNTEVB
  - BJB board: NXP.com/RD772BJBTPLEVB
  - HVBMS reference design bundle using ETPL: NXP.com/RD-HVBMSCTBUN

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